CLAIMS

What is claimed is:

1. An apparatus for controlling cell traffic in a switch platform, the apparatus comprising at least one bidirectional first-in-first-out (FIFO) unit, wherein each bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer, wherein a cell size of the first and second unidirectional FIFO buffers is programmable.

2. The apparatus of claim 1, wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports.

3. The apparatus of claim 1, wherein a word size of the first and second unidirectional FIFO buffers is programmable.

4. The apparatus of claim 1, wherein the at least one bidirectional FIFO unit is coupled to write at least one cell from and read at least one cell to at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, and at least one data interface.

5. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from an ATM interface.

6. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from a frame relay interface.

7. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from a voice interface.

8. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one cell from a data interface.

9. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to read at least one cell to at least one switch, wherein the at least one switch handles cells from sources having a plurality of bandwidths.

A2 Cont.

10. The apparatus of claim 9, wherein the at least one switch is coupled to route the at least one cell to an OC12 trunk line and to at least one service module.

11. The apparatus of claim 10, wherein the at least one service module is coupled to provide the at least one cell to at least one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

12. The apparatus of claim 1, wherein the second unidirectional FIFO buffer is coupled to read at least one cell to an ATM interface.

13. The apparatus of claim 1, wherein the second unidirectional FIFO buffer is coupled to read at least one cell to a frame relay interface.

14. The apparatus of claim 1, wherein the second unidirectional FIFO buffer is coupled to read at least one cell to a voice interface.

15. The apparatus of claim 1, wherein the second unidirectional FIFO buffer is coupled to read at least one cell to a data interface.

16. The apparatus of claim 1, wherein the second unidirectional FIFO buffer is coupled to write at least one cell from at least one switch, wherein the at least one switch handles cells from sources having a plurality of bandwidths.

17. The apparatus of claim 16, wherein the at least one switch is coupled to route the at least one cell from an OC12 trunk line and from at least one service module.

18. The apparatus of claim 17, wherein the at least one service module is coupled to provide the at least one cell to at least one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

19. The apparatus of claim 1, wherein the at least one bidirectional FIFO unit comprises a diagnostic interface, wherein the diagnostic interface supports a non-destructive read of the at least one bidirectional FIFO unit while at least one cell is being written to and read from the at least one bidirectional FIFO unit.

20. The apparatus of claim 1, wherein the at least one cell is written to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer over a first enabled diagnostic loop.

21. The apparatus of claim 1, wherein the at least one cell is written to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

22. The apparatus of claim 1, wherein each unidirectional FIFO buffer outputs a write port cell count, wherein a write port of each unidirectional FIFO buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one more cell.

23. The apparatus of claim 22, wherein at least one master bidirectional FIFO unit ceases reading at least one cell to a unidirectional FIFO buffer of at least one slave bidirectional FIFO unit in response to the write port cell count, wherein the at least one master bidirectional FIFO unit disables at least one switch from routing at least one cell to the at least one slave bidirectional FIFO unit in response to the write port cell count, wherein the at least one switch routes the at least one cell to another of the at least one slave bidirectional FIFO units in response to the write port cell count.

24. The apparatus of claim 23, wherein the at least one master bidirectional FIFO unit resumes reading the at least one cell to the second unidirectional FIFO buffer of the at least one slave bidirectional FIFO unit in response to the write port cell count, wherein the at least one master bidirectional FIFO unit enables at least one switch to route at least one cell to the at least one slave bidirectional FIFO unit in response to the write port cell count.

25. The apparatus of claim 1, wherein each unidirectional FIFO buffer outputs a read port cell count, wherein a read port of each unidirectional FIFO

A2 Cont.

buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one more cell.

Sub E1

26. The apparatus of claim 2, wherein the write port logic of each unidirectional FIFO buffer is synchronous with a write clock.

27. The apparatus of claim 26, wherein the write clock operates at a frequency substantially equal to 50 megahertz.

28. The apparatus of claim 26, wherein the read port logic of each unidirectional FIFO buffer is synchronous with a read clock.

29. The apparatus of claim 28, wherein the read clock operates at a frequency substantially equal to 21 megahertz.

30. The apparatus of claim 28, wherein the read clock operates at a frequency substantially equal to 42 megahertz.

Sub A3

31. The apparatus of claim 1, wherein at least one invalid cell can be discarded from each unidirectional FIFO buffer.

Sub E1

32. The apparatus of claim 1, wherein the switch platform comprises two switches.

Sub A4

33. The apparatus of claim 1, wherein the switch platform comprises at least one service module and at least one cell bus controller, wherein the at least one cell bus controller is coupled among the at least one service module

and at least one switch, wherein the at least one service module comprises at least one slave bidirectional FIFO unit, and wherein the at least one cell bus controller comprises at least one master bidirectional FIFO unit.

34. A network switch platform comprising:

at least one service module;

at least one cell bus controller coupled among the at least one service module and at least one switch;

at least one bidirectional first-in-first-out (FIFO) unit located in the at least one service module and the at least one cell bus controller, wherein each bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer, wherein a cell size of the first and second unidirectional FIFO buffers is programmable;

at least one diagnostic interface, wherein the at least one diagnostic interface supports a non-destructive read of the at least one bidirectional FIFO unit while at least one cell is being written to and read from the at least one bidirectional FIFO unit; and

at least one discard enable signal, wherein at least one invalid cell can be discarded from the at least one bidirectional FIFO unit using the at least one discard enable signal.

35. The network switch platform of claim 34, wherein the at least one bidirectional FIFO unit is coupled to write at least one cell from and read at least one cell to at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, and at least one data interface.

36. The network switch platform of claim 34, wherein the at least one cell is written to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer over a first enabled diagnostic loop, wherein at least one cell is written to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

37. The network switch platform of claim 34, wherein each unidirectional FIFO buffer outputs a write port cell count, wherein a write port of each unidirectional FIFO buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one more cell, wherein each unidirectional FIFO buffer outputs a read port cell count, wherein a read port of each unidirectional FIFO buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one more cell.

38. The network switch platform of claim 34, wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports, wherein the write port logic of each unidirectional FIFO buffer is synchronous with a write clock, and wherein the read port logic of each unidirectional FIFO buffer is synchronous with a read clock.

39. The network switch of claim 34, wherein a word size of the first and second unidirectional FIFO buffers is programmable.

40. The network switch platform of claim 34, wherein the at least one bidirectional FIFO unit is coupled to read at least one cell to and write at least one cell from the at least one switch, wherein the switch handles cells from sources having a plurality of bandwidths.

41. The network switch platform of claim 34, wherein the at least one service module is coupled to receive at least one cell from and provide at least one cell to at least one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

42. A method for controlling cell traffic in a switch platform, the method comprising the step of transferring at least one cell among a plurality of ports having a plurality of bandwidths using a bidirectional first-in-first-out (FIFO) unit, wherein the bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer having a programmable cell size.

43. The method of claim 42, further comprising the step of programming the word size of each of the first and second unidirectional FIFO buffers.

44. The method of claim 42, wherein the step of transferring comprises the steps of:

synchronously writing the at least one cell from at least one port to the first unidirectional FIFO buffer; and

synchronously reading the at least one cell from the first unidirectional FIFO buffer to at least one switch, wherein the reading is asynchronous with the writing.

45. The method of claim 42, wherein the step of transferring comprises the steps of:

synchronously writing the at least one cell from at least one switch to the second unidirectional FIFO buffer; and

synchronously reading the at least one cell from the second unidirectional FIFO buffer to the at least one port, wherein the reading is asynchronous with the writing.

46. The method of claim 42, further comprising the steps of:

discarding at least one invalid cell from each unidirectional FIFO buffer; and

executing a non-destructive read of the at least one bidirectional FIFO unit while at least one cell is being written to and read from the at least one bidirectional FIFO.

47. The method of claim 42, further comprising the steps of:

writing at least one cell to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer using a first enabled diagnostic loop; and

writing at least one cell to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

48. The method of claim 42, further comprising the steps of:

outputting a write port cell count from each unidirectional FIFO buffer;

outputting from a write port of each unidirectional FIFO buffer a status indicating space available in the unidirectional FIFO buffer for at least one more cell;

outputting a read port cell count from each unidirectional FIFO buffer; and

outputting from a read port of each unidirectional FIFO buffer a status indicating space available in the unidirectional FIFO buffer for at least one more cell.

49. The method of claim 42, wherein the plurality of ports comprise at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, at least one data interface, at least one network switch interface, at least one OC12 interface, and at least one OC3 interface.

add C4

add S1

add F1